REMARKS

In accordance with the foregoing, claims 1, 11 and 10 have been amended. Claims 9 and 16 have been cancelled.

Claims 1, 8, 10-15 and 17-19 are pending and under consideration.

STATUS OF CLAIMS

Claims 1, 2, 5, 6, 8, 9, 11, 12 and 16 are rejected.

Claims 3, 4, 7, 10, 13-15, 17 and 18 are objected to.

Claim 19 is allowed.

ITEM 2: REJECTION OF CLAIMS 1, 2, 5, 6, 8, 11, AND 12 FOR OBVIOUSNESS UNDER 35 U.S.C. §103(a) OVER KIM (U.S. PATENT 6,211,867) IN VIEW OF TANAKA (U.S. PATENT, 5,438,290)

The rejection is respectively traversed, for the reasons set forth in the following.

In accordance with independent claims 1 and 11, as amended hereinabove, a first phase adjusting circuit is provided in correspondence with a first output device and a second phase output device. (An illustration of this recited circuit structure of claim 1 is shown in FIG. 7). According to this arrangement, the timing of a changing edge of a driving signal which drives a first output device and the timing of a changing edge of a driving signal which drives a second output device can be independently adjusted. This feature is clarified in the amended independent claims 1 and 11. According to this feature, power consumption can be reduced and malfunctions or erroneous discharge can be improved. (See the description on page 10, lines 1-13).

As emphasized in the interview of May 20, 2003 (see continuation sheet PTOL-413 attached to the outstanding Office Action), applicants' counsel urged, and it is believed that the Examiner agreed, that Kim (U.S. patent 6,211,867) does not disclose a phase adjusting circuit that adjusts timing of a changing edge of a driving signal. Therefore, it is submitted to be apparent that Kim does not disclose a feature of the present invention that first and second phase adjusting circuits are respectively provided in correspondence with first and second output devices.

The Examiner newly urges at page 3 of the Office Action that Tanaka (U.S. Patent 5,438,290) discloses a phase adjustment circuit that adjusts timing of a changing edge of a driving circuit. However, it is respectively submitted that Tanaka does not disclose the feature of the present invention that first and second phase adjusting circuits are respectively provided in correspondence with first and second output devices.

Tanaka discloses a control logic circuit to adjust a timing of switching operations in association with a variable number of terminals required to be driven by various display data. The control logic circuit is designated by numeral 22 in FIG. 7 and the detailed structure of the control logic circuit is shown in FIG. 9. In FIG. 7, pairs of PMOS and NMOS transistors respectively correspond to the first and second output devices of the present invention. Each pair of the PMOS and NMOS transistors is driven by a signal output from a 64 bit latch circuit 25 which is controlled by the control logic circuit 22. The signal is applied to the PMOS transistor via a level converter wherein the signal is applied to the NMOS transistor directly. In other words, each pair of the PMOS and NMOS transistors is driven by the same signal. Further, no phase adjusting circuit is provided on a path from the 64 bit latch circuit 25 to the PMOS transistor and no phase adjusting circuit is provided on a path from the 64 bit latch circuit 25 to the NMOS transistor. Therefore, it is impossible to independently adjust the timings of changing edges of the PMOS and NMOS transistors. According to Tanaka, when the control logic circuit changes the timing of switching operations, the PMOS and NMOS transistors change on and off timings thereof in the same way because they are driven by the same signal.

Alternatively, Tanaka does not disclose or suggest the feature of the present invention that the first and second phase adjusting circuits are respectively provided.

LACK OF *PRIMA FACIE* DEMONSTRATION OF OBVIOUSNESS OF THE COMBINATION

The combination of Kim and Tanaka is merely asserted to have been "obvious to one having ordinary skill in the art ..." without any *prima facie* demonstration of such obviousness, rendering the rejection without basis (MPEP 2142 to 2143.03) and the same accordingly should be withdrawn.

ITEM 4: REJECTION OF CLAIMS 9 AND 16 FOR OBVIOUSNESS UNDER 35 U.S.C. §103(a) OVER MARCOTTE (U.S. PATENT 5,642,018) IN VIEW OF BARCLAY (U.S. PATENT 4,594,588)

This rejection is rendered moot by the above cancellation of the referenced claims.

CONCLUSION

It is respectfully submitted that foregoing has shown that the pending claims herein patentably distinguish over the reference of record and, there being no other objections or rejections, that the application is condition for allowance, which action is earnestly solicited.

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If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

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